REMARKS

Applicant respectfully asks for reconsideration of both this application and the final Office Action dated August 12, 2005.

A response to this Office Action was due by November 12, 2005. Applicant filed a Notice of Appeal on February 12, 2006, together with a Petition for a three month extension of time. Further, Applicant is concurrently submitting a Petition for a four month extension of time and a Request For Continued Examination with this Amendment. Accordingly, Applicant respectfully asks that this Amendment be considered as timely filed.

Applicant again gratefully thanks the Examiner for the personal interview granted with the undersigned on July 5, 2006. This Amendment is presented in accordance with the substance of that interview. In particular, claim 1 is amended herein to incorporate the subject matter of claim 3 (it is believed that claim 1 already had been amended to incorporate the subject matter of claim 2), and claims 2 and 3 have been canceled. Claims 4-7 are then amended to depend from claim 1. Based upon the personal interview with the Examiner, it is believed that these amendments place claims 1 and 4-7 in immediate condition for allowance.

In the outstanding Office Action, claims 1-24 again were rejected under 35 U.S.C. §103 over EPO Patent Application No. EP 1 043 662 A1 to Boles in view of U.S. Patent No. 6,377,911 to Sample et al., in further view of U.S. Patent No. 6,282,503 to Okazaki et al. Applicant courteously repeats his traversal of this rejection, and asks for its reconsideration.

As noted above, Applicant respectfully submits that claims 1 and 4-7 are now in immediate condition for allowance. With regard to claims 14-19, these claims are directed to an

emulator that serializes and then deserializes data to transfer that data from a first logic device to a second logic device during a circuit emulation process. To further emphasize the subject matter of these claims (as distinguished from the subject matter of the Boles, Sample et al. and Okazaki et al. patent documents), claims 14-19 were previously amended to recite that the first programmable logic device is configured to emulate a first partition of a circuit, and the second programmable logic device is configured to emulate a second partition of the circuit. Claims 8-13 and 20-24 similarly recite a method of emulating a circuit by serializing and then deserializing data transferred from a first logic device to a second logic device during the circuit emulation process. Applicants again submit that no combination of the Boles application, the Sample et al. patent and the Okazaki et al. patent would teach or suggest these features of the invention.

Simply put, none of the Boles, Sample et al. or Okazaki et al. patent documents teaches or suggests using the recited serializer, cross point switch and deserializer to actually emulate a circuit. For example, the portion of the Sample et al. patent relied upon by the Examiner is directed to the initial configuration of programmable gate arrays so that these arrays can later be used to perform an emulation process. It does not teach or suggest the use of a serializer or deserializer during the emulation process itself (i.e., once the programmable gate arrays have been configured). Similarly, the portion of the Okazaki et al. patent relied upon by the Examiner discusses the difficulties in initially configuring an emulation circuit as a circuit design changes. This portion of the Okazaki et al. also does not address the use of such a switch in an emulation process after the emulation circuits have been properly configured. The Boles application is then

completely unrelated to an emulation process, and instead discusses a generalized technique for allowing a function circuit 12 to have access to multiple pin locations at point P1 and P2.

Accordingly, Applicant again respectfully submits that no combination of the Boles application, the Sample et al. patent and the Okazaki et al. patent would teach or suggest these features of the invention recited in any of claims 1-24. It is therefore again urged that the rejection of these claims over the combination of the Boles application, the Sample et al. patent and the Okazaki et al. patent be withdrawn.

The Commissioner is authorized to charge any fees that may be necessary to maintain the pendency of this application, including any fees under 37 C.F.R. §1.16 or §1.17, to Deposit Account No. 19-0733.

Applicant respectfully submits that all of the claims are allowable, and that this application therefore is in condition for allowance. Applicant courteously asks for favorable action regarding this Amendment at the Examiner's earliest convenience

Respectfully submitted,

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